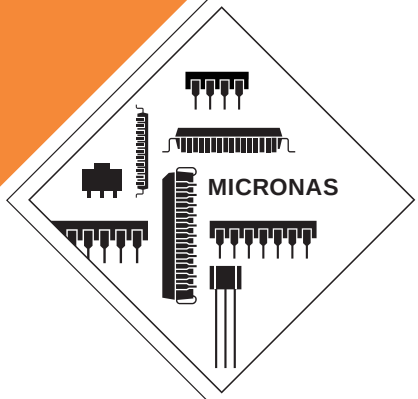


DATA SHEET

UAC 3553B
Universal Serial Bus (USB) DAC

Edition Feb. 17, 2005
6251-595-2DS

MICRONAS

Contents

Contents, continued

Universal Serial Bus (USB) DAC

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The UAC 3553B is a fully integrated 2-channel audio digital-to-analog converter (DAC) with an integrated USB 2.0 full-speed interface controller.

The device offers audio processing such as volume, bass, and treble. Furthermore, the UAC 3553B integrates a programmable 5-band parametric equalizer for correcting the frequency response of the applied speakers. Integrated headphone amplifiers allow direct headphone connection.

The DAC is driven by digital audio input via a USB Audio Class-compliant isochronous stream 16 or 24 bits wide or via an I^2S input 16 or 32 bits wide. Both audio input data can be fully mixed to the DAC output. The integrated high-quality DSP-based adaptive sample rate converter accepts USB audio streams in a wide range from 6.4 to 48 KHz.

General-purpose inputs and outputs connect the UAC 3553B to peripheral hardware such as buttons, keyboards, LEDs, etc. USB HID Device class for audio controls is supported. Over an I^2C master, more complex peripherals, such as LCD displays can be controlled; and the UAC 3553B itself can be remote-controlled via I^2C slave operation. This allows communication pipelining between a peripheral I^2C system controller and the USB host.

All-in-all, the IC is designed as the ideal connecting matrix between USB, digital audio input, home stereo, and all kinds of human interface devices. Many functions are adjustable to the customer's needs. Moreover, firmware customizing and plug-in download functionality to the on-chip microcontroller turns the UAC 3553B into a customer-specific IC. Micronas supplies a standard ROM firmware based on the USB Composite Class, Audio Class, and HID Class.

Table 1–1: Members of the UAC 355xB family

Version	Description
UAC 3553B	USB DAC
UAC 3554B	USB headset
UAC 3555B	USB codec
UAC 3556B	USB codec-emulator version with additional 8 k RAM for program download.

1.1. Features

- single-chip, USB specification 2.0 compliant, stereo audio D/A converter
- supports up to 24-bit playback
- optional vendor identification and device configuration with external EEPROM
- bus-powered and self-powered mode possible
- remote wake-up
- 8 general-purpose input/output pins with HID support
- I^2S input interface
- independent adaptive sample rates of 6.4 to 48 kHz for USB playback
- audio baseband control: bass, treble, loudness, volume, balance, and mute
- dynamic bass management Micronas Bass (MB)
- digital speaker equalizer (5-band parametric equalizer)
- THD better than −90 dB and SNR of typical 96 dB for D/A converters
- power supply rejection ratio >95 dB for analog outputs
- integrated stereo headphone amplifier
- I^2C interface (master/slave)
- customized firmware extensions possible with plug-ins

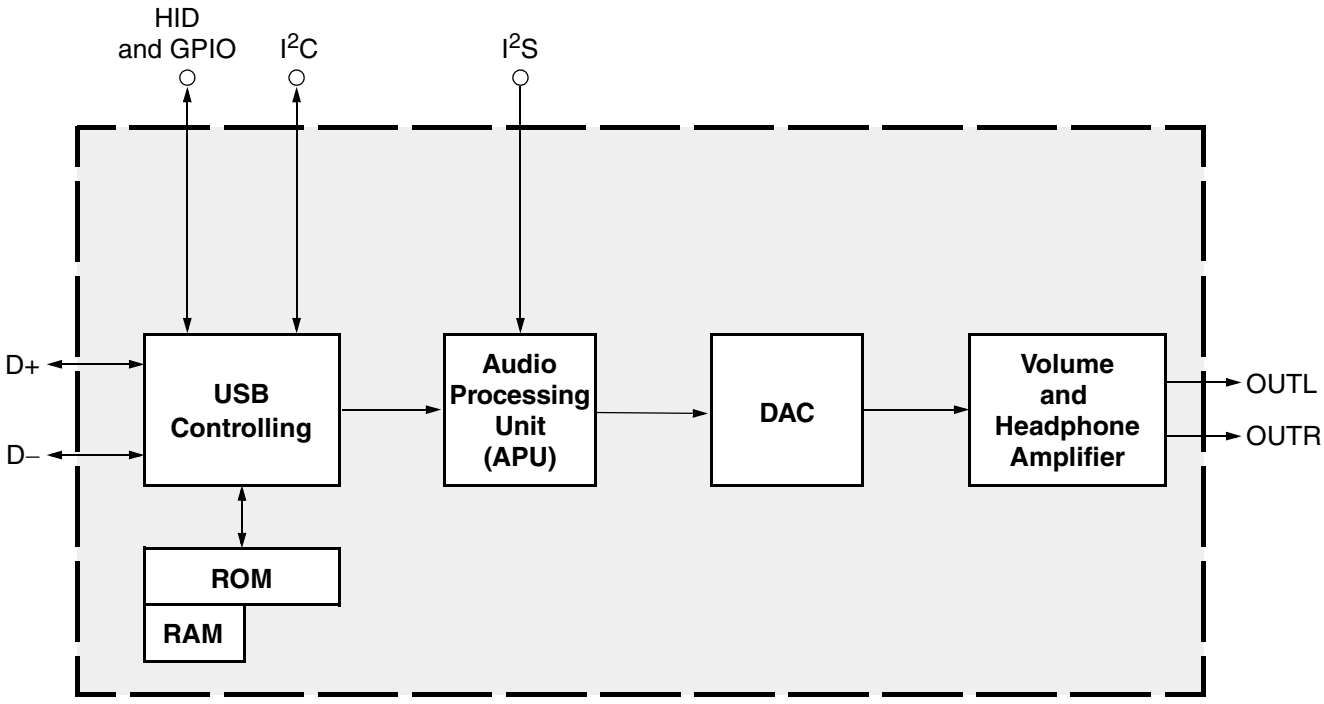


Fig. 1–1: Block diagram of the UAC 3553B

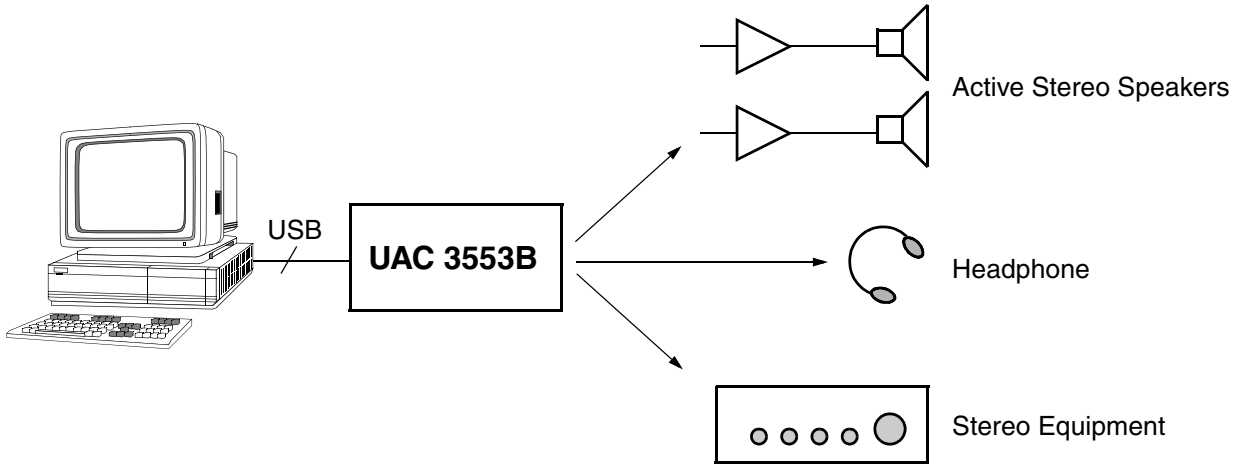


Fig. 1–2: System application diagram

2. Hardware Description

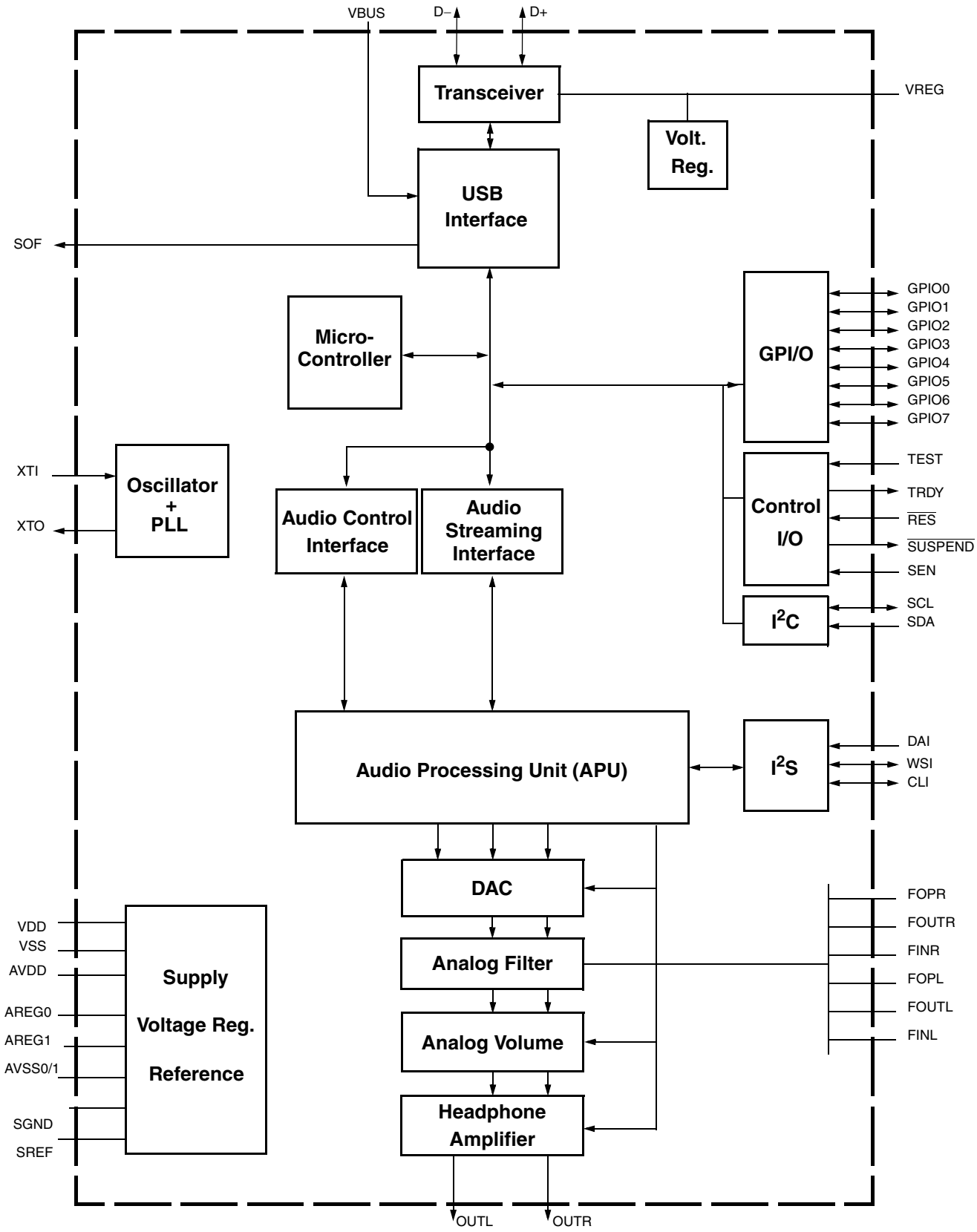


Fig. 2–1: Detailed block diagram of the UAC 3553B

2.1. General Information

This description summarizes all hardware platform capabilities of the UAC 3553B. The functionality for a certain application, however, is defined in the microcontroller's firmware. This is explained in Section 4. "Firmware" on page 16.

The basic functions (playback, audio control, HID) of the UAC 3553B can entirely be used by any USB operating system without additional drivers.

However, the IC offers far more functions if vendor-specific controlling or download code is used. With external I^2C controlling, the IC can even work as an audio DAC in a non-USB environment. The use of this complete functionality is not described in the standard data sheet and can be found in separate application notes (www.micronas.com).

A detailed block diagram of the UAC 3553B is depicted in Fig. 2–1. The functions of the blocks are explained in the following sections.

2.2. Universal Serial Bus (USB)

2.2.1. Transceiver

The differential input transceiver is used to handle the USB data signal according to the full-speed (12 MB/s) USB driver characteristics (USB SPEC 2.0). This block is supplied by an internal voltage regulator. The internal pull-up resistor on the D+ line, indicating that the UAC 3553B is connected to the USB bus, can be switched on and off by firmware.

2.2.2. USB Interface

The USB interface does all the low-level USB protocol handling, like NRZI coding, bit-stuffing and CRC computation. A receiver/transceiver logic handles the data traffic between the USB bus and the microcontroller memory.

2.2.3. Microcontroller

The microcontroller is an 8-bit RISC controller which handles the USB Chapter-9 processing and the decoding of class and vendor-specific USB requests. Detailed information is available in a separate document. The basic configuration is:

– 2 KB RAM

– 12 KB ROM

A part of the RAM is reserved for download plug-ins. This allows the addition of smaller portions of code to the basic firmware for extended functionality or serves as a patch area. One example is adding extra functions to the GPIO pins, like control of external components via USB. Downloading of the plug-in can be done either from the USB host with an extra driver or from an external I^2C EEPROM.

2.3. GPIO

The pins GPIO0…GPIO7 can be switched into different electrical states:

– input, output, or tristate

– weak or strong driver strength

– internal pull-down on or off

2.4. General-Purpose Timer

The UAC 3553B incorporates a timer. It is a 16-bit counter with clock prescaler. The clock runs at 12 MHz. The prescaler can be set to divide by 1 to 256.

The current value of the counter can always be read back.

The timer initiates interrupts on reaching the count value MaxA.

The structure of the timer is shown in Fig. 2–2.

Timer frequency:

$$\left(T_{CLK} = \frac{12MHz}{Prescale}\right)$$

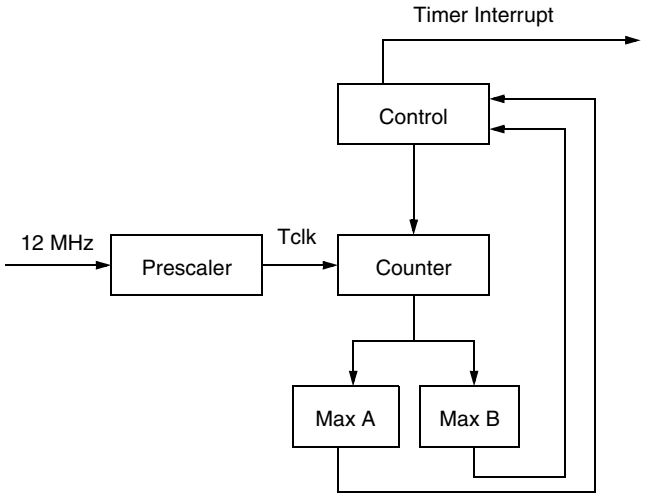


Fig. 2–2: Timer structure

2.5. Audio Streaming Interface

The audio streaming interface directly connects the USB interface to the APU in order to transmit the digital audio data for playback. The following data formats are supported:

Table 2–1: Audio formats

Playback
16-bit MONO
16-bit STEREO
24-bit STEREO

2.6. Audio Control Interface

The audio control interface links the microcontroller to the APU and is used to initialize the APU and to transmit audio-related USB control data, such as volume setting, tone control, etc.

The audio control interface provides full access to all APU registers via the microcontroller.

2.7. I^2S Interface

Used Pins: DAI, WSI, CLI

The I^2S interfaces operate in 16-bit or 32-bit mode. Delayed word strobe or standard I^2S format can be selected via programmable delay bit. Word strobe polarity is also programmable.

2.7.1. Asynchronous I^2S input

Used Pins: DAI, WSI, CLI

In this mode the UAC 3553B is slave, i.e., asynchronous input is possible at a sampling rate range from 6.4 kHz to 48 kHz. The external I^2S source provides DAI, WSI, and CLI

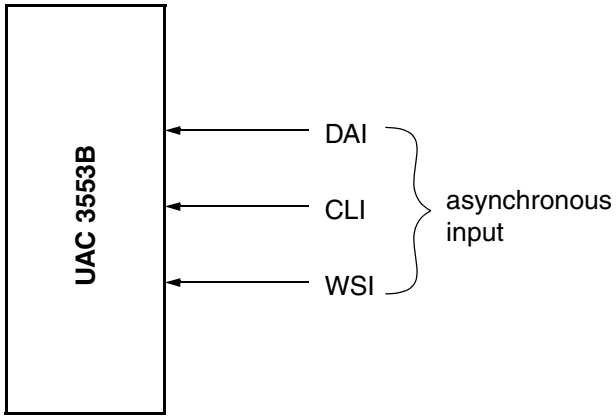


Fig. 2–3: Asynchronous I^2S input

2.7.2. Synchronous I^2S Input Mode

Used Pins: DAO, DAI, WSI, CLI

In this mode external digital sources use CLI and WSI as reference and generate synchronous input data on DAI.

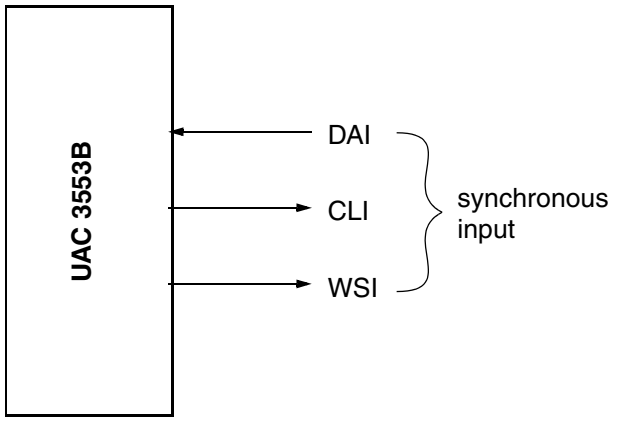


Fig. 2–4: Synchronous I^2S input

2.8. Power Supply

The UAC 3553B has on-chip voltage regulators providing the optimal supply voltages for the analog and digital sections, thus allowing to power the IC by the USB bus supply lines, as well as from external supply. They are also used to reduce cross-talk and EMI.

For stable operation, all regulators need external capacitors.

The regulators are

1. VREG:
   3.4 V Regulator for USB signalling (saving external regulator)
2. AREG0:
   3.5 V regulator for analog back-end
3. AREG1:
   3.5 V regulator for analog circuitry apart from back-end.

Reference voltage for analog signals:

SREF:
1.7 V (optional 2.3 V) reference voltage for analog circuitry.

Note: It is recommended to connect AVSS0/1, SGND and VSS. In certain applications, however, it may be better to split signal ground from the other grounds in order to reduce noise.

Five-Volt Mode

If a higher output level is required, the IC can operate in 5 V mode. In this case, the IC is powered from an external 5 V supply: AVDD has to be connected to AREG0 and AREG1 and SREF must be switched to 5 V mode.

2.9. I^2C Bus Interface

Pins: SDA, SCL

The UAC 3553B is equipped with an I^2C bus master/slave interface. The bus format and timing follows the original specification for I^2C (The I^2C Specification V2.1). It operates with 5 V signaling at 100 kHz or 400 kHz.

Both master and slave mode require support from the microcontroller firmware.

2.9.1. I^2C Master

This mode allows control of external I^2C devices, such as EEPROMs, LCD-Displays etc. This interface is used to download configuration data and firmware from an EEPROM after power-up. The bus protocol (subaddressing and packet length) is defined by firmware, and so is programmable.

Note: Micronas standard firmware (Section 4. “Firmware” on page 16) provides support for USB-to-I^2C bridging, allowing control of I^2C devices via USB.

2.9.2. I^2C Slave

In I^2C slave mode, the interface provides an interrupt to the microcontroller after detecting the assigned I^2C address (0x48). The corresponding interrupt service routine handles this request and interprets incoming data according to the application.

One example of handling could provide full access to all memory locations.

2.10. Analog Output

Pins: OUTL, OUTR,
FOPL, FOPR, FOUTL, FOUTR, FINL, FINR

The analog output system comprises the stereo audio DAC, analog filters, op amps for external out-of-band-noise filters, analog volume, mute, and the output amplifiers.

2.10.1. Digital-to-Analog Converters

The UAC 3553B uses two multibit sigma delta DACs with high linearity and SNR better than 95 dBA.

2.10.2. Analog Filter

Pins: FOPL, FOPR, FOUTL, FOUTR, FINL, FINR

This block contains the op-amps for the optional analog external out-of-band-noise filters. It is recommended to use a second-order filter for the main channels (OUTL, OUTR) (see Section 4. “Firmware” on page 16). It is possible to omit these filters and to save the external components. In this case, the op-amp has to be switched off and the pins FOOTL/R, FINL/R and FOPL/R must be connected. The output signal will contain more out-of-band noise, which is not audible, however.

2.10.3. Analog Volume

The analog volume covers a range from +6 dB to −18 dB with 1.5 dB step size. But this is the analog component of the overall volume system which covers a range from +12 dB to −114 dB with 1 dB step size and additional mute position. It is split into analog and digital volume. This splitting ensures that the DAC performance parameters do not degrade at reduced volume settings. The splitting is embedded in the audio processing and cannot be modified.

Note: Positive volumes will degrade the THD at high input levels.

2.10.4. Line-out/Headphone Amplifier

Pins: OUTL, OUTR

Stereo Mode

The line-out/headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or to a power amplifier. The stereo headphones require external serial resistors in both channels. See Section 4. “Firmware” on page 16.

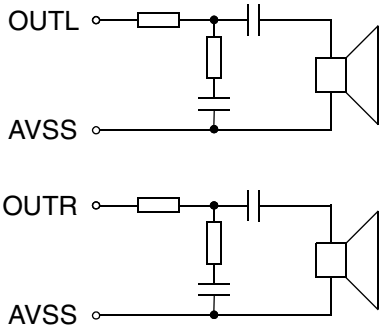


Fig. 2–5: Loudspeaker connection for stereo mode

Mono Mode

In Mono mode, the DC coupling capacitors and further filter circuitry are not required. In this mode, the output pins OUTL/R operate in bridge mode with complementary signals. Therefore, the maximum output power increases allowing small speakers to be driven directly.

Fig. 2–6: Loudspeaker connection for mono mode

2.11.Special I/O

Pins: SOF, SEN, $\overline{\text{SUSPEND}}$, $\overline{\text{RESET}}$

The following sections describe some pins with special functions.

2.11.1.SOF (Start of Frame)

The SOF pin provides a 1 ms periodic signal which is derived from the USB frame rate. It can be used for test purposes or as an USB-synchronous reference for vendor-specific external circuitry.

2.11.2.SEN (Suspend Enable)

Pin: SEN

This is a digital input that prevents the device from entering the low-power mode (Suspend). The UAC 3553B enters a low-power mode if:

– J-state on D+, D– lines (USB-Suspend) and Vbus high

– Vbus low (USB-disconnected)

Note: Both cases must be supported by the firmware

In the case of USB-Suspend, the SEN pin is also used as an input for the remote wake-up function.

Table 2–2: SEN pin

SEN	
high	suspend enabled
low	suspend disabled/remote wake-up

2.11.3. Suspend

Pin: $\overline{\text{SUSPEND}}$

The $\overline{\text{SUSPEND}}$ pin is a digital output pin which indicates the low-power mode. It can be used to power down external circuitry, like power amplifiers in a USB speaker.

Table 2–3: $\overline{\text{SUSPEND}}$ pin

SUSPEND	
high	normal power
low	low power

2.11.4. Reset

Pin: $\overline{\text{RES}}$

The $\overline{\text{RES}}$ pin resets the UAC 3553B. During power up the $\overline{\text{RES}}$ pin should be low until the clock system is up and running. Then this pin can be released and the UAC 3553B enters normal operating mode.

Note: In low-power mode, the RES pin must not be low, to avoid restart of the clock system and thus entrance to normal power mode.

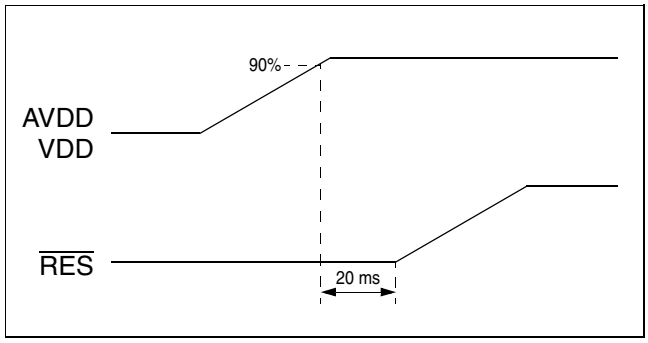


Fig. 2–7: Timing diagram of the reset procedure

2.12.Clock System

Pins: XTI, XTO

The UAC 3553B requires a 12 MHz clock source, which is implemented as an on-chip oscillator with external crystal. Also an external oscillator can be used. In this case, the clock has to be connected to XTI (see also Section 4. “Firmware” on page 16). The 12 MHz is the input clock for a PLL circuit which generates all clocks required within the IC.

The clock for the APU is programmable either to 48 MHz or 72 MHz. With 48 kHz, the UAC 3553B consumes less power, but on the other hand a reduced feature set for the audio processing has to be taken into account (see Fig. 3. on page 12).

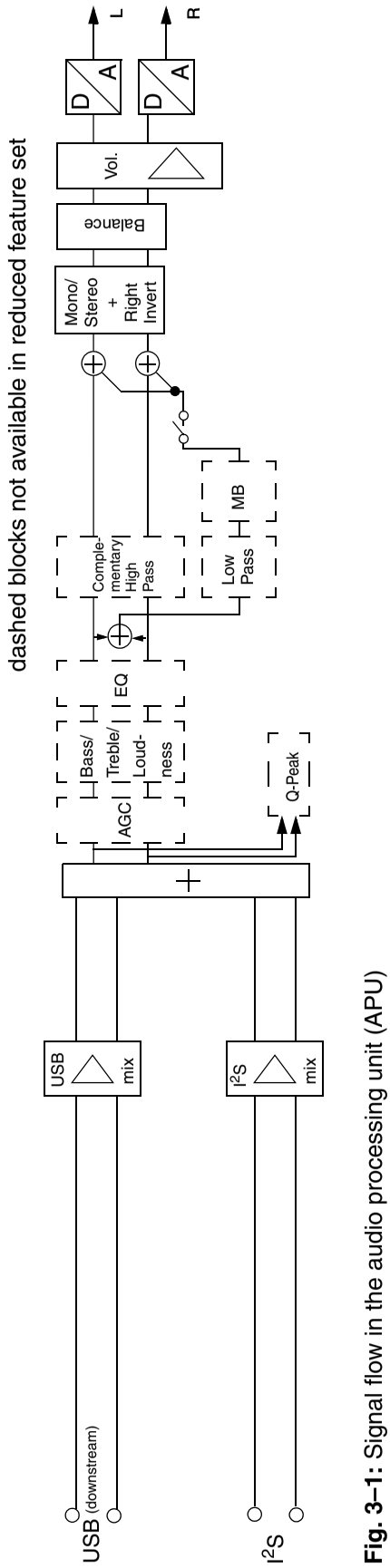


Fig. 3–1: Signal flow in the audio processing unit (APU)

3. Audio Processing

The audio processing is implemented by the APU firmware. The audio building blocks can be split into USB-independent features such as parametric equalizer, I^2S I/O, and blocks which belong to USB feature units, mixer units, and selection units defined in the USB Device Class Definition for Audio Devices.

The USB feature unit provides basic manipulation of the incoming logical channels and can be controlled by the standard OS-provided mixer tool. The parameters for the USB-independent features are predefined in the internal ROM, in an external EEPROM or a special host application which drives the IC.

The UAC 3553B supports two logical channels (i.e., left and right). Multichannel or surround systems, however, can also be realized using more than one UAC 3553B, because phase or delay distortion is eliminated in the device by locking the audio processing to the USB frame rate. An overview of the architecture is given in Fig. 3–1 on page 12.

If the APU works with a 48 MHz clock, it is necessary to select the reduced feature mode. Those blocks not available in reduced feature mode, are shown with dashed lines in Fig. 3–1 on page 12.

3.1. Sample Rate Converters

The tasks for the sample rate converters are:

– to transform the block-transferred audio on the USB bus into a continuous data stream and vice versa,

– to convert all incoming and outgoing sample rates to and from a fixed 48 kHz sample rate.

This technique eliminates input and output data jitter. Furthermore, all audio algorithms, the ADCs, and the DACs run on a single sample rate and no parameter switching is required on change of audio sampling rate. The sample rate converters support input and output sampling rates from 6.4 kHz up to 48 kHz.

3.2. Automatic Gain Control

The Automatic Gain Control (AGC) is one of the building blocks of the feature unit (USB Device Class Definition for Audio Devices 1.0, page 39).

Different sound sources fairly often do not have the same volume level. The Automatic Gain Control solves this problem by equalizing the volume levels within a defined range. Below a threshold level the signals are not affected. The level-adjustment is performed with time constants in order to avoid short-time adjustments due to signal peaks.

Table 3–1: AGC parameters

Parameter	Settings	Default
Decay time	8 s 4 s 2 s 20 ms	4 seconds

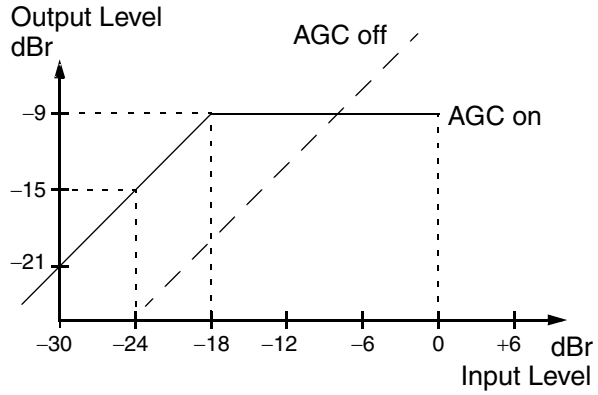


Fig. 3–2: Simplified AGC characteristics

3.3. Quasi-Peak

A quasi-peak detector is provided in the DAC channel. This can be used, e.g., for a VU-meter on the host side.

The feature is based on using the following fast attack and slow decay time constants:

attack time: 1.3 ms

decay time: 37 ms

3.4. Bass Control

The bass control provides gain or attenuation to frequency components below a cut-off frequency of 120 Hz. The bass control works identically on both channels in a range of –12 dB to +12 dB.

3.5. Treble Control

The treble control provides gain or attenuation to frequency components above a cut-off frequency of 6 kHz. The treble control works identically on both channels in a range from –12 dB to +12 dB.

3.6. Parametric Equalizer

The parametric equalizer is an audio feature which is not accessed via standard USB controls. It allows the compensation of the frequency response of a speaker. Alternatively, frequency responses can be set to suit individual tastes. The equalizer consists of five individually adjustable bands. The control parameters and the parameter range for each band is shown in Table 3–2.

Table 3–2: Equalizer parameters

Parameter	Min.	Max.
Center Frequency	50 Hz	15 kHz
Gain/Attenuation	−6 dB	+6 dB
Filter Quality (Q)	0.5	3

The adjustment of the equalizer is supported by an application program that allows setting up frequency responses and downloading the corresponding filter coefficients into the UAC 3553B. When the frequency response matches the requirements, it can be programmed into the external EEPROM or can be set by a vendor-specific device driver. The UAC 3553B is shipped with a flat frequency response.

3.7. Volume, Mute, and Balance Control

The volume control is partly implemented in the analog back-end. This preserves high audio quality (SNR) at low volume settings because signal and noise are attenuated in the same way. This is a significant advantage over digital-only implementations since it preserves the native audio bit resolution in the processing path. The UAC 3553B uses digital volume control only for the fine stepping. The volume setting is smoothed by an internal ramping algorithm in order to avoid audible clicks during volume change. The splitting between analog and digital volume is handled by the UAC 3553B automatically.

The balance is implemented digitally by attenuating one channel.

The mute control is part of the volume system in the UAC 3553B. It functions simultaneously on both channels and can be switched on and off under USB control. Similar to the volume control, clicks are avoided by a ramping algorithm.

3.8. Micronas Bass (MB)

The Micronas bass algorithm (MB) implements a sophisticated bass boost system, which extends the frequency range of loudspeakers or headphones.

The MB is placed in the crossover filter path. The enhanced bass signal can be added back onto the left/right channels. Micronas bass combines two effects: dynamic amplification and adding harmonics.

Several parameters allow tuning the characteristics of MB according to the loudspeaker, the cabinet, and personal preferences. For more detailed information on how to set up MB, Micronas provides an appropriate Application Note.

Table 3–3: MB parameters

Parameter	Range	Default if disabled	Default if enabled
Effect Strength	off to max.	off	medium
Harmonic Content	0 to 100%	0%	50%
Center Frequency	20 to 300 Hz	90 Hz	90 Hz
Amplitude Limit	−32 to 0 dBFS	0 dBFS (= no limit)	0 dBFS (= no limit)

3.8.1. Dynamic Amplification

Since the human impression of loudness depends on the frequency, a dynamic compression of the low frequencies adapts the sound to the human perception.

In order to prevent clipping, and to adapt the system to the signal amplitude which is really present at the output of the device, the MB contains a definable limit. The output signal amplitude is monitored and if it comes close to the limit, the gain is reduced automatically. Clipping effects are avoided.

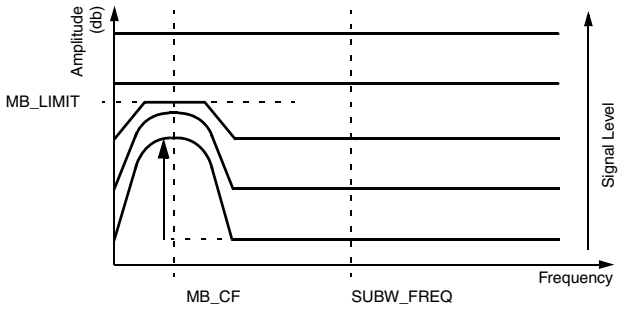


Fig. 3–3: Dynamic amplification

3.8.2. Adding Harmonics

MB exploits the psychoacoustic phenomenon of the 'missing fundamental'. Adding harmonics of the frequency components below the cut-off frequency gives the impression of actually hearing the low-frequency fundamentals. In other words: Although the loudspeaker system is not capable of generating such low frequencies, the listener has the impression that it reproduces them.

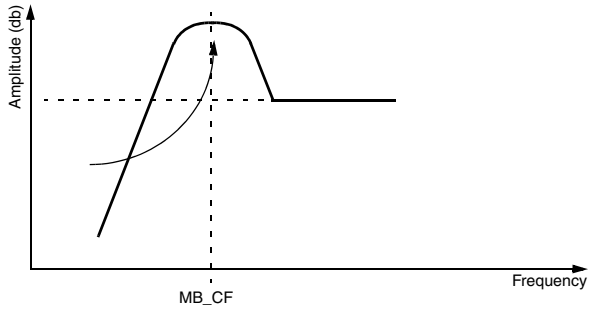


Fig. 3–4: Adding harmonics

4. Firmware

It was the purpose of the previous chapters to describe the UAC 3553B from the hardware point of view. The complete functionality, however, is defined by the microcontroller firmware. This firmware tailors the device to a specific application. Micronas offers a standard DAC firmware version which is embedded in the ROM.

Note: By means of an external EEPROM, it is possible to customize many parameters (IDs, strings, equalizer setting etc.).

4.1. Features

The main features of the standard firmware versions are

- USB playback with sample rates from 6.4 kHz to 48 kHz
- Audio baseband processing including dynamic bass management
- Basic audio control by GPIO-HID
- Suspend mode and remote wake-up support
- I²C master/slave support
- bootloader allows download of configuration data, plug-ins after power-on
- plug-in support (downloadable firmware extensions from external EEPROM or WIN driver)

Most of the functionality is defined in the device and configuration descriptor. The following chapters provide all noteworthy information buried in this descriptor. It is assumed that the reader is familiar with the basic USB notation (USB Spec 1.1 etc.).

4.1.1. Device Descriptor

The device descriptor contains the downloadable IDs and the index for the strings.

Table 4–1: Programmable device descriptor items

Item	Default - UAC 3553B
idVendor	0x074D
idProduct	0x3553
bcdDevice	0x000x[1)]
iManufacturer	0x01
iProduct	0x02
iSerialNumber	0x00
[1)] changes with new firmware revisions	

Associated to the string index there are three programmable strings. The ROM firmware defines only two:

Table 4–2: Strings used in DAC firmware

String	Default - UAC3553B
Manufacturer String	Micronas
Product String	UAC3553B USB-DAC

4.1.2. Configuration Descriptor

First the configuration descriptor contains information on the bus/self-powered and remote wake-up capabilities. The UAC 3553B allows all combinations of these features. There is also a string index, allowing to associate a string to this configuration. The default string is the date code (time of code assembly). These items are programmable.

Table 4–3: Programmable configuration descriptor Items

Item	Default - UAC3553B
iConfig	0x01
bmAttributes	0xC0 (self-powered, remote wake-up
MaxPower	0x00 (0mA)

Then the configuration descriptor provides all information concerning the audio flow in the Class Specific Audio Control Interface. Fig. 4–1 shows the graphical representation for the DAC firmware.

This is the audio structure as it appears to the USB host. Without any additional drivers, the Windows OS provides sliders in the mixing tool to control volume, bass, treble setting. Using a vendor-specific application, however, it is possible to extend this to the full signal routing capabilities (see Section 3. on page 12). This can be achieved by plug-ins from external EEPROM or Windows driver.

Note: BassBoost enables a dynamic bass management algorithm with programmable (external EEPROM) characteristics.

The next part of the configuration descriptor defines the audio format for playback. This is not programmable.

Table 4–4: Supported audio formats

Playback Format
16-bit MONO
16-bit STEREO
24-bit STEREO

The UAC 3553B accepts all sample rates from 6.4 kHz to 48 kHz

The last part of the configuration descriptor defines the HID functions:

The DAC firmware uses the GPIO pins to connect keys which are related to the USB HID class. The standard configuration defines the GPIO0...GPIO7 as input pins for the audio and media control shown in Table 4–5.

Table 4–5: Standard key configuration

Pin	Function
GPIO0	Volume Up
GPIO1	Volume Down
GPIO2	Mute on-off toggle
GPIO3	BassBoost on-off toggle
GPIO4	Next Track
GPIO5	Previous Track
GPIO6	Stop
GPIO7	Playback

The keys are polled every 1 ms by the microcontroller and the corresponding key codes are transmitted to the host on request when a key enters high state. The host's polling rate is 8 ms. This parameter, however, is part of the configuration set, which can be downloaded from an external I^2C EEPROM.

If these HID functions are not required, the GPIO[0...7] can be used as general-purpose I/O by vendor-specific applications.

4.1.3. Audio Class Requests

The DAC firmware supports all audio class requests which are required by the standard audio flow shown in Fig. 3–1. The MIN/MAX/RES setting follows the limits which are defined in the audio processing, apart from the main volume setting (FU1). In this case, the overall range from −114 dB to +6 dB is limited to −40 dB to +3 dB (plus mute position) in order to fit the audible range to the volume slider in the Windows mixer.

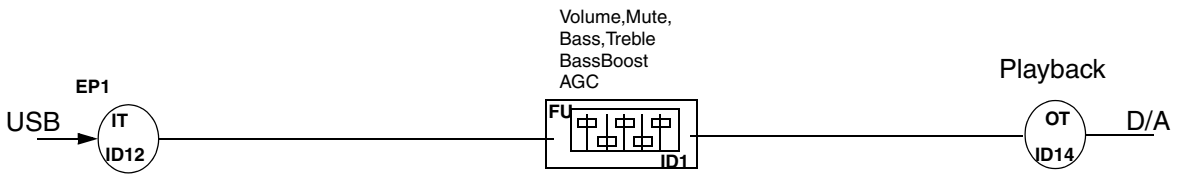


Fig. 4–1: Standard DAC audio flow

4.2. Vendor-Specific Requests

These requests provide functionality which extends standard controlling of the operating system. Micronas provides a driver for the Windows operating system which supports:

– SET MEM
This request allows writing all RAM and register locations in the chip.

– GET MEM
This request allows reading all memory locations in the chip. Block read is supported.

– SET I^2C
This vendor request allows to drive the I^2C-master in the DAC firmware. It allows writing to external I^2C devices.

– GET I^2C
This request supports I^2C master reading from external devices.

4.2.1. Bootloader

The bootloader is a part of the firmware which allows communication with an external I^2C EEPROM. In multimaster applications with I^2C control, however, it is not allowed to have I^2C traffic coming from UAC 3553B and therefore, the bootloader needs to be enabled by GPIO7:

Table 4–6: Bootloader enable

Setting	Bootloader
GPIO7 = 0	disabled
GPIO7 = 1	enabled

The bootloader runs immediately after power-on. At this moment, the device is not connected to the USB bus.

When the bootloader has finished, the pull-up resistor is switched on the D+ line to signal to the host that the device is ready for enumeration. If no external EEPROM is found, the UAC 3553B continues with the default configuration. Two I^2C EEPROM types with different I^2C device IDs and number of subaddresses are supported and can be selected by GPIO6. The EEPROM type and size must be chosen according to the content.

Table 4–7: Supported I^2C EEPROM types

GPIO6	Device ID	Sub-addresses	Size	Purpose
1	0x51	1 Byte	<2 kbit	Configuration (and very small plug-ins)
0	0x50	2 Bytes	>2 kbit	Configuration and plug-ins

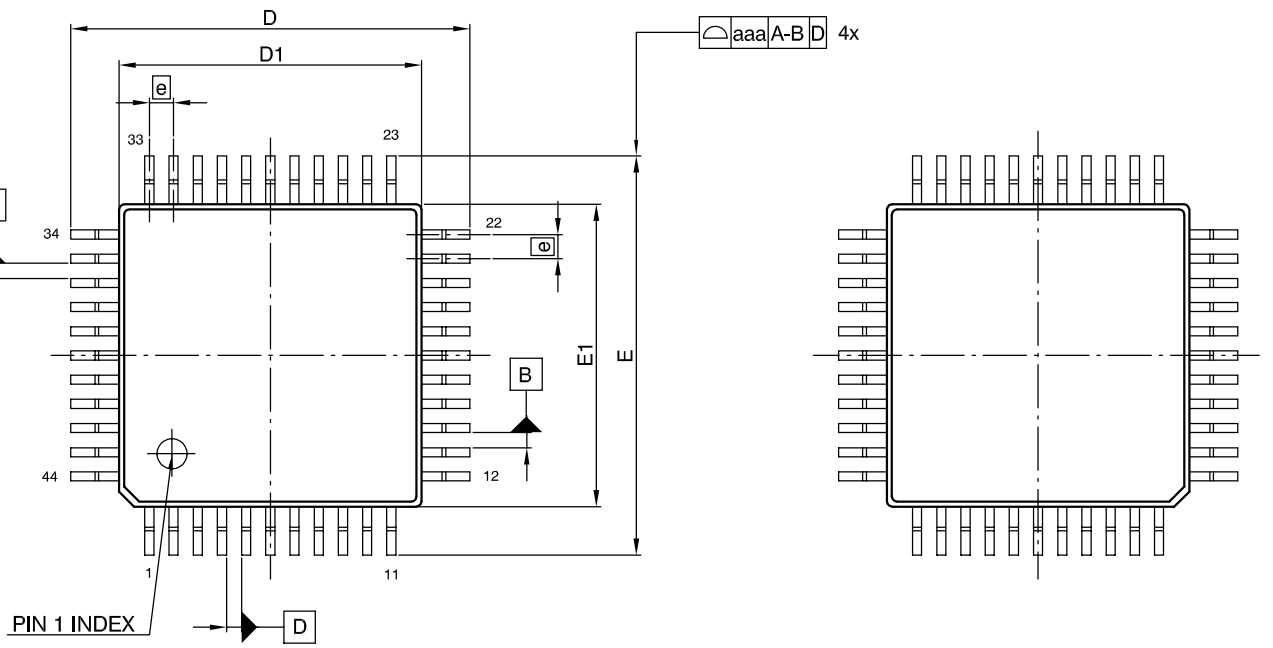
The size of the EEPROM must be chosen according to the content.

Details on the EEPROM content and the structure of the different sections can be found in separate application notes.

Using GPIO6/7 as bootloader option bits may cause conflicts with the use of these pins as HID media control pins. In this case, a plug-in or a hardware workaround is available.

5. Specifications

5.1. Outline Dimensions



UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.45 0.29	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.8	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-01-23	06599.0001.4	SPZG001003_001_02

Fig. 5–1:
PMQFP44-1: Plastic **M**etric **Q**uad **F**lat **P**ackage, **44** leads, 10 × 10 × 2 mm^3
Ordering code: QG
Weight approximately 0.5 g

5.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS
OBL = obligatory; connect as described in circuit diagram
VDD = connect to VDD

Pin No. PMQFP 44-1	Pin Name	Type	Connection (If not used)	Short Description
1	XTI	IN	OBL	Quartz Oscillator Pin 1
2	XTO	OUT	OBL	Quartz Oscillator Pin 2
3	AREG1	OUT	OBL	Regulator Output for analog parts except amplifiers
4	AVSS1/AVSS0	IN	OBL	VSS for analog parts
5	OUTL	OUT	LV	Audio Output: headphone left/speaker Left
6	OUTR	OUT	LV	Audio Output: headphone right/speaker Right
7	AREG0	OUT	OBL	Regulator Output for audio output amplifiers
8	AVDD	IN	OBL	analog VDD
9	DAI	IN	VSS	I^2S Data Input
10	WSI	IN/OUT	VSS	I^2S Word Strobe
11	CLI	IN/OUT	VSS	I^2S Bit Clock
12	GPIO 7	IN/OUT	LV	HID IO 7
13	GPIO 6	IN/OUT	LV	HID IO 6
14	GPIO 5	IN/OUT	LV	HID IO 5
15	GPIO 4	IN/OUT	LV	HID IO 4
16	GPIO 3	IN/OUT	LV	HID IO 3
17	GPIO 2	IN/OUT	LV	HID IO 2
18	GPIO 1	IN/OUT	LV	HID IO 1
19	GPIO 0	IN/OUT	LV	HID IO 0
20	SDA	IN/OUT	LV	I^2C Data
21	SCL	IN/OUT	LV	I^2C Clock
22	TRDY	OUT	LV	Test Output Pin
23	VBUS	IN	OBL	Sense USB Bus
24	VREG	OUT	OBL	Capacitor for internal supply
25	DMINUS	IN/OUT	OBL	USB DATA MINUS
26	DPLUS	IN/OUT	OBL	USB DATA PLUS
27	VSS	IN	OBL	Digital VSS
28	VDD	IN	OBL	Digital VDD

Pin No. PMQFP 44-1	Pin Name	Type	Connection (If not used)	Short Description
29	TEST	IN	VSS	Test Enable
30	$\overline{\text{RES}}$	IN	VDD	Power On Reset, active low
31	$\overline{\text{SUSPEND}}$	OUT	LV	Low-Power Mode Indicator
32	SOF	OUT	LV	1-ms Start-Of-Frame Signal
33	SEN	IN	VSS	Suspend Enable
34	FOUTL	OUT	OBL	Output to left external filter
35	FOPL	IN/OUT	OBL	Filter Op Amp Inverting Input, left
36	FINL	IN/OUT	OBL	Input for FiltoutL
37	FOUTR	OUT	OBL	Output to right filter op amp
38	FOPR	IN/OUT	OBL	Right Filter op amp inverting input
39	FINR	IN/OUT	OBL	Input for FILTOUTR
40	NC		LV	Leave Vacant
41	NC		LV	Leave Vacant
42	SGND	IN	OBL	Signal Reference Ground
43	SREF	IN	OBL	Signal Reference Voltage
44	NC		LV	Leave Vacant

5.3. Pin Descriptions

5.3.1. Power Supply Pins

The UAC 3553B combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD (28)
VSS (27)
The VDD and VSS power supply pair are connected internally with all digital parts of the UAC 3553B.

AVDD (8)
AVDD is the supply pin for the voltage regulators at AREG0(9) and AREG1(4).

AVSS0/1 (4)
AVSS1 is the ground connection for the analog audio processing parts, including the headphone/loudspeaker amplifiers.

SREF (43)
Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against SGND with a 3.3 µF capacitor.

Note: The pin has a typical DC level of 1.725 V. It can be used as reference input for external op amps when no current load is applied.

SGND (42)
Reference ground for the internal band-gap and biasing circuits. **This pin should be connected to a clean ground potential!** Any external distortions on this pin will affect the analog performance of the UAC 3553B.

AREG0 (7)
Voltage regulator output for headphone/loudspeaker amplifiers supply. Connect an external ceramic capacitor to stabilize the regulator output.

AREG1 (3)
Voltage regulator output for analog audio processing parts supply, except the headphone/loudspeaker amplifiers. Connect an external ceramic capacitor to stabilize the regulator output.

5.3.2. Analog Audio Pins

FOUTL (34)
FOPL (35)
FINL (36)
FOUTR (37)
FOPR (38)
FINR (39)

Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R pins are directly connected with the inputs of the inverting filter op amps. The FINL/R pins are connected to the outputs of the op amps.

OUTL (5)
OUTR (6)
These pins are connected to the internal output amplifiers. OUTL/R can be used for either line-out or stereo headphones.

Note: Warning: A short-circuit at these pins for more than a momentary period may result in destruction of the internal circuits!

5.3.3. Interface Pins

DMINUS (25)
DPLUS (26)
Differential USB port pins. The DPLUS pin has an internal switchable pull-up resistor. Both pins must be connected to the USB bus via a series resistor.

VBUS (23)
Sense USB Bus.

CLI (11)
Clock line for the I^2S bus. This line is driven by the UAC 3553B; in slave mode, an external I^2S clock has to be supplied.

DAI (9)
Input of digital serial sound data to the UAC 3553B via I^2S bus.

WSI (10)
Word strobe line for the I^2S bus. In master mode, this line is driven by the UAC 3553B; in slave mode, an external I^2S word strobe has to be supplied.

SDA (20)
Via this pin, the I^2C bus data is written to or read from the UAC 3553B.

SCL(21)
Via this pin, the I^2C bus clock signal has to be supplied.

5.3.4. Other Pins

XTI (1)
XTO (2)
The XTI pin is connected to the input of the internal crystal oscillator; the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors (see application diagram).

Note: Do not drive external clock circuits via XTI/XTO!

SEN (33)
Digital input that prevents the device from entering the low-power mode. This pin is also used to signal remote wake-up.

TEST (29)
Test enable. This pin is for test purposes only and must always be connected to VSS.

VREG (24)
Voltage regulator output for USB transceiver supply. Connect an external ceramic capacitor to stabilize the regulator output.

$\overline{\text{RES}}$ (30)
A LOW signal at this pin resets the chip.

GPIO 0…7
(19, 18, 17, 16, 15, 14, 13, 12)
These pins are configurable to either being input or output and can be used to connect audio function keys or signalling LEDs.

$\overline{\text{SUSPEND}}$ (31)
This pin indicates that the host PC sets the USB bus to the suspend mode state.

SOF(32)
Start of Frame Signal. 1 ms signal that can be used for external application circuits.

TRDY (22)
Test Output Pin. This pin is intended for test purposes only and must not be connected.

5.4. Pin Configuration

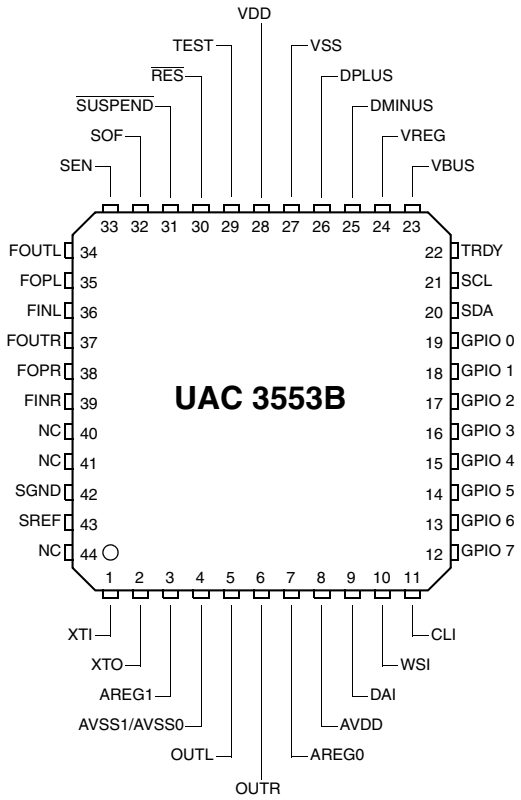


Fig. 5–2: PMQFP44-1 package

5.5. Pin Circuits

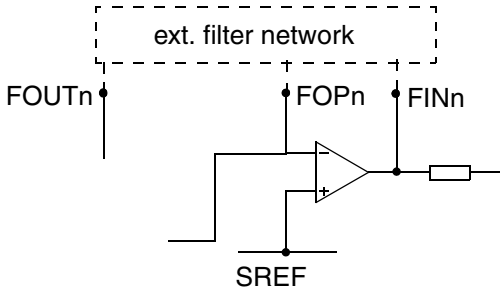


Fig. 5–3: Pins FINR, FOPR, FINL, FOPL

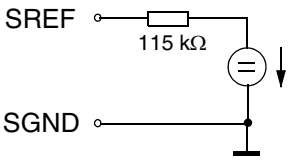


Fig. 5–4: Pins SREF, SGND

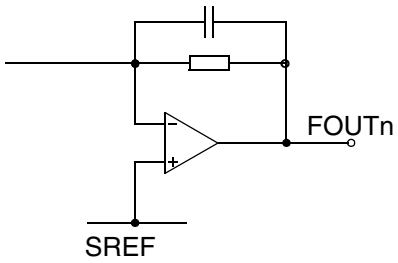


Fig. 5–5: Output pins FOUTL, FOUTR

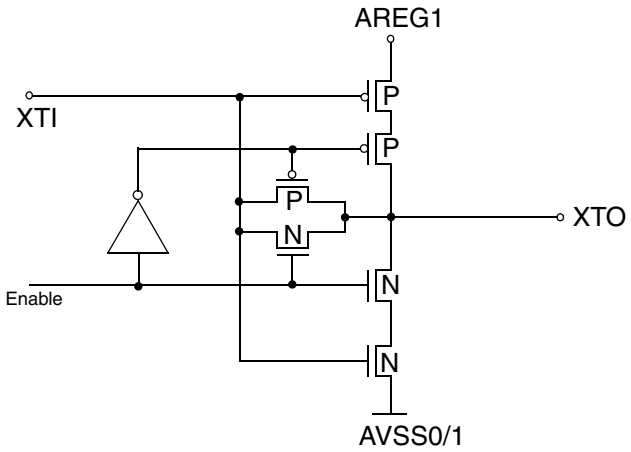


Fig. 5–6: Clock oscillator XTI, XTO

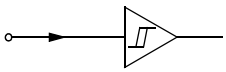


Fig. 5–7: Input pins $\overline{\text{RES}}$, TEST, SEN, DAI

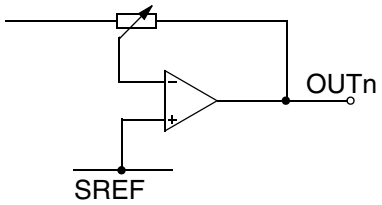


Fig. 5–8: Output pins OUTL, OUTR

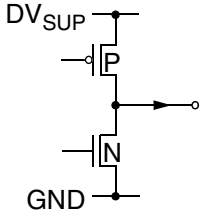


Fig. 5–9: Digital output pins SOF, $\overline{\text{SUSPEND}}$, TRDY

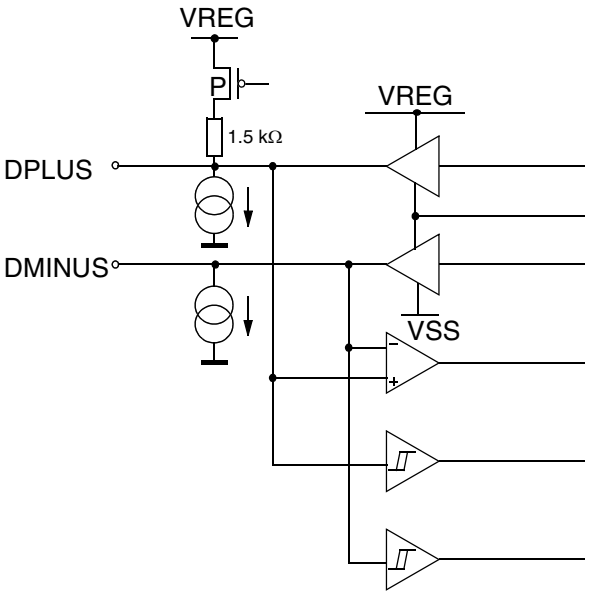


Fig. 5–10: Digital input/output pins DMINUS, DPLUS, VREG

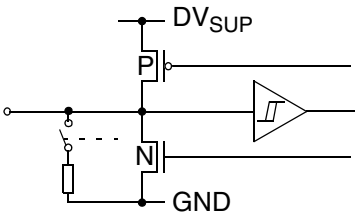


Fig. 5–11: Input/output pins GPIO0 ... GPIO7, WSI, CLI

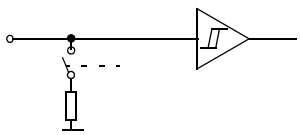


Fig. 5–12: Input pin VBUS

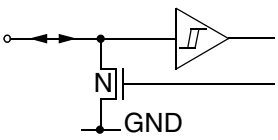


Fig. 5–13: Input/output pins SDA, SCL

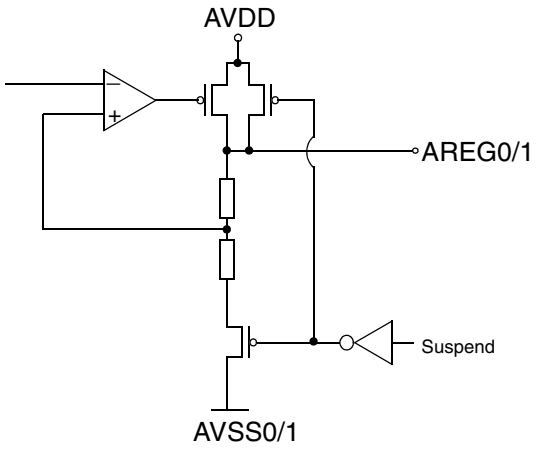


Fig. 5–14: Analog voltage supply pins AVDD, AVSS, AREG0/1

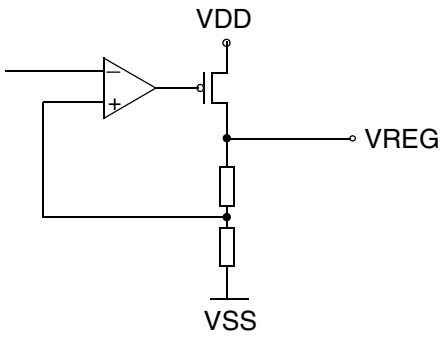


Fig. 5–15: Digital voltage supply pins VDD, VSS, VREG

5.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

5.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground ($V_{SUPA,}$ V_{SUPDx} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in Section 2.8. of this document.

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A	Ambient Operating Temperature		–10	70	°C
T_C	Case Operating Temperature PMQFP44-1		–10	115[3)]	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Power Dissipation PMQFP44-1		–	760[3)]	mW
V_{SUPA}	Analog Supply Voltage [1)]	AVDD	–0.3	6	V
V_{SUPA}	Analog Supply Voltage [2)]	AVDD, AREG0/1	–0.3	6	V
V_{SUPDx}	Digital Supply Voltage	VDD	–0.3	6	V
ΔV_{GRND}	Voltage Differences between different Grounds	AVSS0, AVSS1, VSS	–0.5	+0.5	V
V_{Idig}	Input Voltage, all digital inputs		–0.3	V_{SUPD} + 0.3	V
I_{Idig}	Input Current, all digital inputs		–20	+20	mA
I_{Odig}	Output Current, all digital outputs		–50	+50	mA
V_{Iana}	Input Voltage, all analog inputs		–0.3	$V_{VAREG0/1}$+ 0.3	V
I_{Iana}	Input Current, all analog inputs		–5	+5	mA

1) Internal regulators used
2) If internal regulators are not used, connect AVDD to AREG0/1.
3) Package limit.

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
I_{Oaudio}	Output Current, audio output[1)]	OUTL/R	−0.2	0.2	A
I_{AREG0}	Output Current, analog regulator	AREG0	−500	+20	mA
I_{AREG1}	Output Current, analog regulator	AREG1	−50	+20	mA
[1)] These pins are **not** short-circuit proof!					

5.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground ($V_{SUPA,}$ V_{SUPDx} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in section Section 2.8. of this document.

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature Range		0	25	70	°C
T_C	Case Operating Temperature PMQFP44-1			65	110	°C
P_{MAX}	Power Dissipation PMQFP44-1				650 mW	°C
V_{SUPA}	Analog Audio Supply Voltage	AVDD	4.1	5.0	5.6	V
C_{SUPA}	Capacitor at analog supply pins to ground	AVDD		220		nF
V_{SUPD}	Digital Supply Voltage	VDD	4.1	5.0	5.6	V
C_{SUPD}	Capacitor at digital supply pin to ground	VDD		100		nF
C_{SUPUSB}	Capacitor at VBUS pin to ground	VBUS		22		nF
Analog Reference						
C_{SREF1}	Analog Reference Capacitor	SREF	1	3.3		µF
C_{SREF2}	Ceramic Capacitor in parallel	SREF		100		nF
Analog Audio Filter Inputs and Outputs						
Z_{AFLO}	Analog Filter Load Output[1)]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Analog Filter Load Input[1)]	FINL/R	5.0		7.5	kΩ pF
Analog Audio Outputs						
Z_{AOL_HP}	Output Load Headphone (16 Ω series resistor required)	OUTL/R	16	32 100		Ω pF

[1)] Please refer to Section 6. “UAC 3553B Applications” on page 38

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
Crystal Characteristics[1]						
T_{AC}	Ambient Temperature Range		0		70	°C
F_P	Load Resonance Frequency at C_{load} = 15 pF[2]	XTI		12		MHz
V_{ACLK}	Clock Amplitude	XTI, XTO	0.5		V_{REG}–0.5 [1]	V_{PP}
$\Delta F/F_s$	Accuracy of Adjustment		–500		500	ppm
$\Delta F/F_s$	Frequency Variation versus Temperature		–500		500	ppm
R_{EQ}	Equivalent Series Resistance				60	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
P_D	Drive Level				1	mW
Voltage Regulator						
C_{VREG}	Voltage Regulator Capacitor (ceramic, X5R)	VREG	330	1000		nF
C_{AREG0}	Voltage Regulator Capacitor (ceramic, X5R)	AREG0	330	470	600	nF
C_{AREG1}	Voltage Regulator Capacitor (ceramic, X5R)	AREG1	150	220	270	nF
Transceiver						
R_{USB}	Input Series Resistance	DPLUS/ DMINUS		24 (±5%)		Ω

[1] For device characteristics refer to page 31
[2] C_{load} should typically be 15 pF (+30%/–10%), e.g., Y5U. Ref. to application circuit (see Fig. 6–2 on page 39)

5.6.3. Characteristics

At T_A = 0 to 70 °C, V_{SUPD} = 4.1 V to 5.6 V, V_{SUPA} = 4.1 V to 5.6 V. Typical values at T_A = 20 °C, V_{SUPD} = V_{SUPA} = 5.0 V, quartz frequency = 12 MHz, duty cycle = 50%, bass/treble: 0 dB, **M**icronas **B**ass: off, AGC: off, equalizer: off (positive current flowing into the IC), 3 V mode, reduced feature set, if not otherwise specified.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Symbol	**Parameter**	**Pin Name**	**Limit Values**			**Unit**	
I_{VDD}	Current Consumption[1]	VDD		57 45	70	mA	72 MHz APU clock 48 MHz APU clock
				30	80	µA	Suspend
Digital Input Pin							
I_I	Input Leakage Current	GPIO[7:0], SEN, RES, VBUS, DAI, WSI, CLI			±1	µA	$V_{GND} \le V_I \le V_{SUP}$
V_{IL}	Input Low Voltage				0.4	V	
V_{IH}	Input High Voltage		V_{SUPD} −0.4V			V	
Digital Output Pin							
V_{OH}	Output High Voltage	GPIO[7:0], SUSPEND, SOF, WSI, CLI, SDA, SCL	V_{SUPD} −0.4			V	Pins set to output I_{out}=8 mA
V_{OL}	Output Low Voltage				0.4	V	
I_{O_max}	Max. Output Current				1[3] 8[2)3]	mA	output set to “weak” output set to “strong”
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio	AVDD		12	15	mA	all analog blocks on, Mute
				120	135	µA	Suspend
				25		mA	$R_L \ge 32\ \Omega$ (external 16 Ω series resistor required) Volume = 0 dB, Input signal 1kHz at 0 dB_{FS}
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Outputs (internal regulators active)	AVDD, OUTL/R		95		dB	1 kHz sine wave at 100 mV_{rms}
				55		dB	≤ 100 kHz sine wave at 100 mV_{rms}
Analog Supply Voltage Regulators							
V_{AREG}	Output Voltage	AREG0/1, AVSS0/1	3.3	3.5	3.7	V	

1) no load attached to GPIOs
2) max output current for driving LEDs is 20 mA.
3) the sum of these digital output pin currents must not exceed 100 mA. Higher currents might damage the device.

Please consider power limitations due to USB specification.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Reference Frequency Generation							
V_{DCXTI}	DC Voltage at Oscillator Pins	XTI/O		0.5 × V_{Areg1}		V	
C_{LI}	Input Capacitance at Oscillator Pin	XTI		3		pF	
C_{LO}	Input Capacitance at Oscillator Pin	XTO		3		pF	
$V_{XTALOUT}$	Voltage Swing at Oscillator Pins (peak-to-peak)	XTI/O	0.6 × V_{Areg1}		1.0 × V_{Areg1}	V	
T_{OSC_rise}	Oscillator Start-Up Time				10	ms	after min. V_{SUPA} is reached
USB Transceiver							
V_{REG}	Regulator Voltage	VREG	3.25	3.4	3.55	V	C_L=1 µF
R_O	Driver Output Resistance including the 24 Ω external serial resistor	D+/D–	28		43	Ω	static, LOW or HIGH
t_r / t_f	Rise and Fall Times	D+/D–	4		20	ns	C_L=50 pF, driver mode
MA_TRTF	Rise/Fall Time Matching	D+/D–	90		110	%	C_L=50 pF, driver mode
V_{XOVER}	Crossover Voltage	D+/D–	1.3	1.65	2.0	V	C_L=50 pF, driver mode
V_{CM_DREC}	Differential Receiver Common-Mode Range	D+/D–	0.8		2.5	V	
V_{T_SREC}	Single-ended Receiver Threshold Voltage	D+/D–	0.8		2.0	V	
R_{pu}	Switchable Pull-up Resistor	VREG, D+		1.5		kΩ	USB connected
Analog Audio							
V_{SREF}	Signal Reference Voltage	SREF	1.6	1.725	1.8	V	R_L >> 10 MΩ, referred to SGND
V_{AO}	Analog Output Voltage AC	OUTL/R		2.4		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq$ 10kΩ, volume = 0 dB, Input 1 kHz at 0 dB_{FS} digital (I^2S)
R_{inAO}	Analog output resistance[1)]	OUTL/R		3	6	Ω	volume = 0 dB
$PSRR_{A0}$	Power Supply Rejection Ratio	AVDD, OUTL/R		88[1)]		dB	1 kHz sine wave at 100 mV_{rms}
		AVDD, OUTL/R		54[1)]		dB	≤ 100 kHz sine wave at 100 mV_{rms}
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R		0.1[1)]		dB	0...20 kHz (with 2nd order post filter)
$A_{D/A}$	D/A Stop Band Attenuation			40[1)]		dB	31 kHz...164 kHz (with 2nd order post filter)

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
THD_{HP}	Total Harmonic Distortion	OUTL/R		–90	–85	dB	BW = 20 Hz...22 kHz, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
THD_{HP}	Total Harmonic Distortion	OUTL/R		–70		dB	BW = 20 Hz...22 kHz, unweighted, $R_L \geq 32\ \Omega$, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	90	97		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at – 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	95	102		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
USB Transceiver							
V_{REG}	Regulator Voltage	VREG	3.25	3.4	3.55	V	C_L=1 µF
R_O	Driver Output Resistance including the 24 Ω external serial resistor	D+/D–	28		43	Ω	static, LOW or HIGH
t_r / t_f	Rise and Fall Times	D+/D–	4		20	ns	C_L=50 pF, driver mode
MA_TRTF	Rise/Fall Time Matching	D+/D–	90		110	%	C_L=50 pF, driver mode
V_{XOVER}	Crossover Voltage	D+/D–	1.3	1.65	2.0	V	C_L=50 pF, driver mode
V_{CM_DREC}	Differential Receiver Common-mode Range	D+/D–	0.8		2.5	V	
V_{T_SREC}	Single-ended Receiver Threshold Voltage	D+/D–	0.8		2.0	V	
R_{pu}	Switchable Pull-up Resistor	VREG, D+		1.5		kΩ	USB connected
Analog Audio							
V_{SREF}	Signal Reference Voltage	SREF	1.6	1.725	1.8	V	R_L >> 10 MΩ, referred to SGND
V_{AO}	Analog Output Voltage AC	OUTL/R		2.4		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq 10k\Omega$, volume = 0 dB, Input 1 kHz at 0 dB_{FS} digital (I^2S)
R_{inAO}	Analog output resistance[1)]	OUTL/R		3	6	Ω	volume=0 dB
$PSRR_{A0}$	Power Supply Rejection Ratio	AVDD, OUTL/R		88[1)]		dB	1 kHz sine wave at 100 mV_{rms}
		AVDD, OUTL/R		54[1)]		dB	≤ 100 kHz sine wave at 100 mV_{rms}

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R		0.1[1)]		dB	0...20 kHz (with 2nd order post filter)
$A_{D/A}$	D/A Stop Band Attenuation			40[1)]		dB	31 kHz...164 kHz (with 2nd order post filter)
THD_{HP}	Total Harmonic Distortion	OUTL/R		–90	–85	dB	BW = 20 Hz...22 kHz, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
THD_{HP}	Total Harmonic Distortion	OUTL/R		–70		dB	BW = 20 Hz...22 kHz, unweighted, $R_L \geq 32\ \Omega$, Volume = 0 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	90	97		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = 0 dB, Input 1 kHz at – 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	95	102		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10k\Omega$, Volume = –40 dB, Input 1 kHz at –3 dB_{FS} digital (I^2S)
Lev_{Mute}	Mute Level L/R	OUTL/R		–110		dB	BW = 20 Hz...22 kHz unweighted, no digital input signal, Volume = Mute
P_{HP}	Output Power (Speaker/Headphone)	OUTL/R		10		mW_{eff}	$R_L = 32\ \Omega$, 16 Ω series resistance, Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
P_{HP}	Output Power in Bridge Mode (Mono Speaker/Headphone)	OUTL/R		180		mW_{eff}	$R_L = 16\ \Omega$, no series resistors, right channel inverted and output set to mono (bridge mode) Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
VOL_{AO}	Output Volume Setting Range	OUTL/R	–90		0	dB	
$dVOL_{AO}$	Output Volume Step Size	OUTL/R		1		dB	
VOL_{GA}	Output Volume Error	OUTL/R	–0.5	0	0.5	dB	
VOL_{dGA}	Analog Output Volume Step Size Error	OUTL/R	–0.5	0	0.5	dB	
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTL/R		–95	–80	dB	$R_L = 32\ \Omega$, 3 V Mode, Volume = 0 dB, Input = –3 dB_{FS} digital (I^2S)

[1)] not tested in production

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Different Characteristics in Five-Volt Mode							
V_{SREF}	Signal Reference Voltage	SREF	2.25	2.3	2.35	V	$R_L >> 10$ MΩ, referred to SGND
V_{AO}	Analog Output Voltage AC	OUTL/R		3.2		V_{pp}	BW = 20 Hz...22 kHz, $R_L \geq 10$ kΩ, volume = 0 dB, Input 1 kHz at −3 dB_{FS} digital (I^2S)
THD_{HP}	Total Harmonic Distortion	OUTL/R		−93	−85	dB	BW = 20 Hz...22 kHz, $R_L \geq 10$kΩ, Volume = 0 dB, Input 1 kHz at −3 dB_{FS} digital (I^2S)
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	90	99		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10$kΩ, Volume = 0 dB, Input 1 kHz at − 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	95	109		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10$kΩ, Volume = −40 dB, Input 1 kHz at −3 dB_{FS} digital (I^2S)
P_{HP}	Output Power (Speaker/Headphone)	OUTL/R		17		mW_{eff}	$R_L = 32$ Ω, 16 Ω series resistance, Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
P_{HP}	Output Power in Bridge Mode (Mono Speaker/Headphone)	OUTL/R		320		mW_{eff}	$R_L = 16$ Ω, no series resistors, right channel inverted and output set to mono (bridge mode) Volume = 0 dB, Input = 0 dB_{FS} digital (I^2S)
[2)] related to 0 dB_{FS} input level							
Different Characteristics for Full Feature Set (see Fig. 2–1 on page 6), Three-Volt Mode							
SNR_{AO1}	Signal-to-Noise Ratio[2)]	OUTL/R	88	95		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10$kΩ, Volume = 0 dB, Input 1 kHz at − 20 dB_{FS} digital (I^2S)
SNR_{AO2}	Signal-to-Noise Ratio[2)]	OUTL/R	93	100		dB(A)	BW = 20 Hz...22 kHz, A-weighted, $R_L \geq 10$kΩ, Volume = −40 dB, Input 1 kHz at −3 dB_{FS} digital (I^2S)
[2)] related to 0 dB_{FS} input level							

5.6.4. I2S Interface Timing Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{s_I2S}	I^2S Input Setup Time before Rising Edge of Clock	CLI DAI	10			ns	
t_{h_I2S}	I^2S Input Hold Time after Rising Edge of Clock		40			ns	
t_{d_I2S}	I^2S Output Delay Time after Falling Edge of Clock	CLI WSI			30	ns	C_L=30 pF
t_{o_I2S}	I^2S Output Setup Time before Rising Edge of Clock	CLI	4			ns	C_L=30 pF

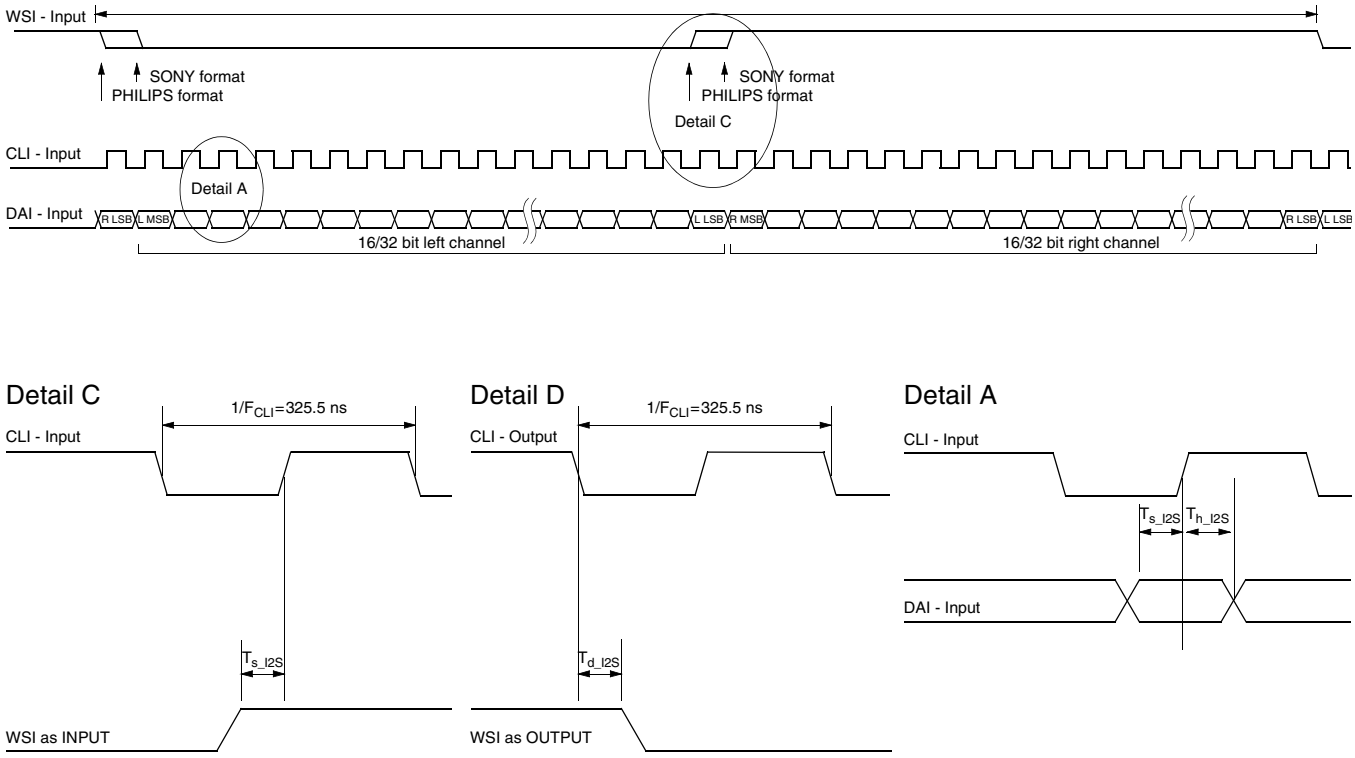


Fig. 5–16: Timing: asynchronous I^2S input

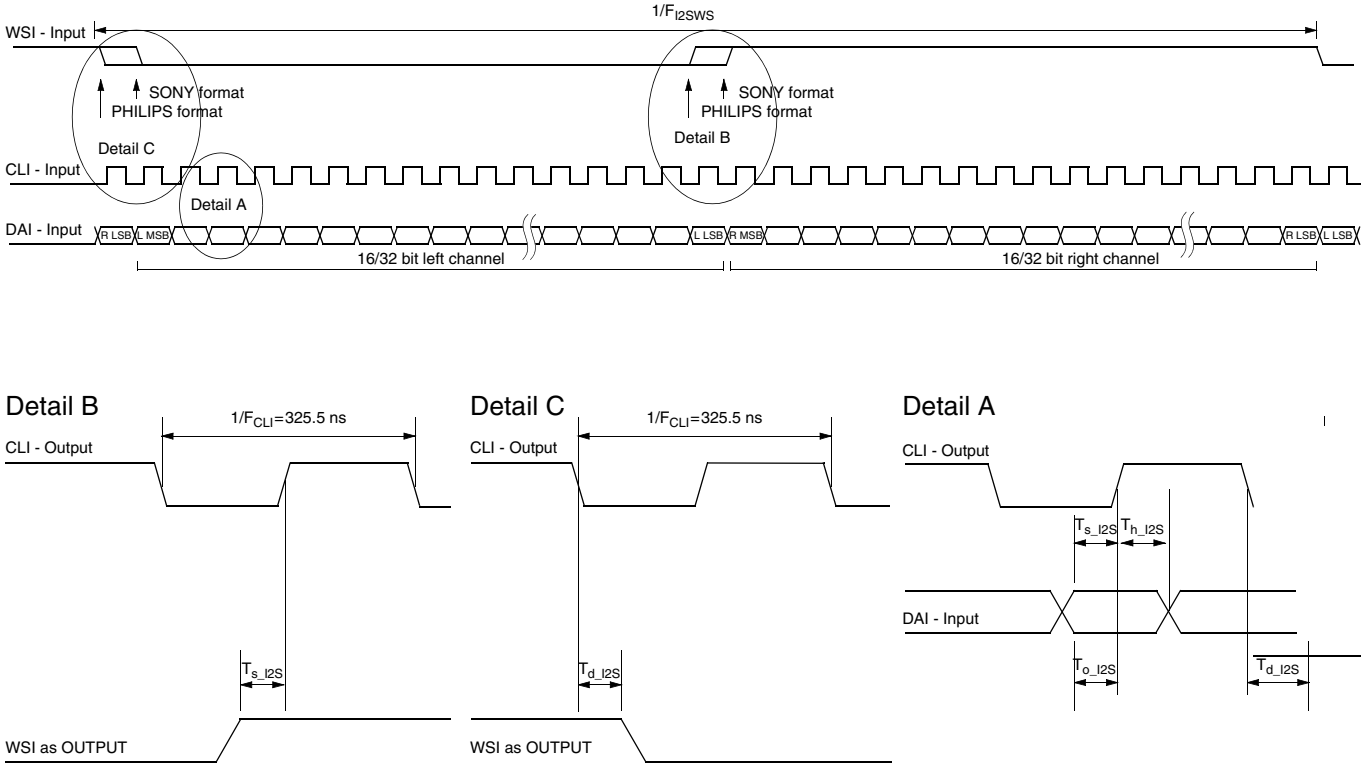


Fig. 5–17: Timing: synchronous I²S input

6. UAC 3553B Applications

6.1. Recommended Low-Pass Filters for Analog Outputs

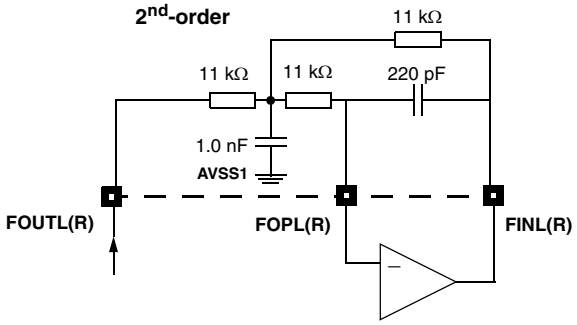


Fig. 6–1: 2nd-order low-pass filter

If the filter is not used, then FOUTL(R), FOPL(R), and FINL(R) are to be connected (dashed line) and the internal op-amp must be switched off.

Table 6–1: Attenuation of second-order low-pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB

Note: First or third-order low-pass is also possible, but then the frequency response degrades.

6.2. External Clocking via XTI

AC coupling of the clock signal

The input level should be in the range between 0.5 and 2.5 V_{PP} for a load capacitance of 22 pF at XTO.

DC coupling of the clock signal

The DC input level must be 0.5 × V_{AREG1} which is typically 1.75 V. The input level should not exceed 0.5 to 2.5 V_{PP}.

See also Section 2.12. on page 11.

6.3. Typical Application

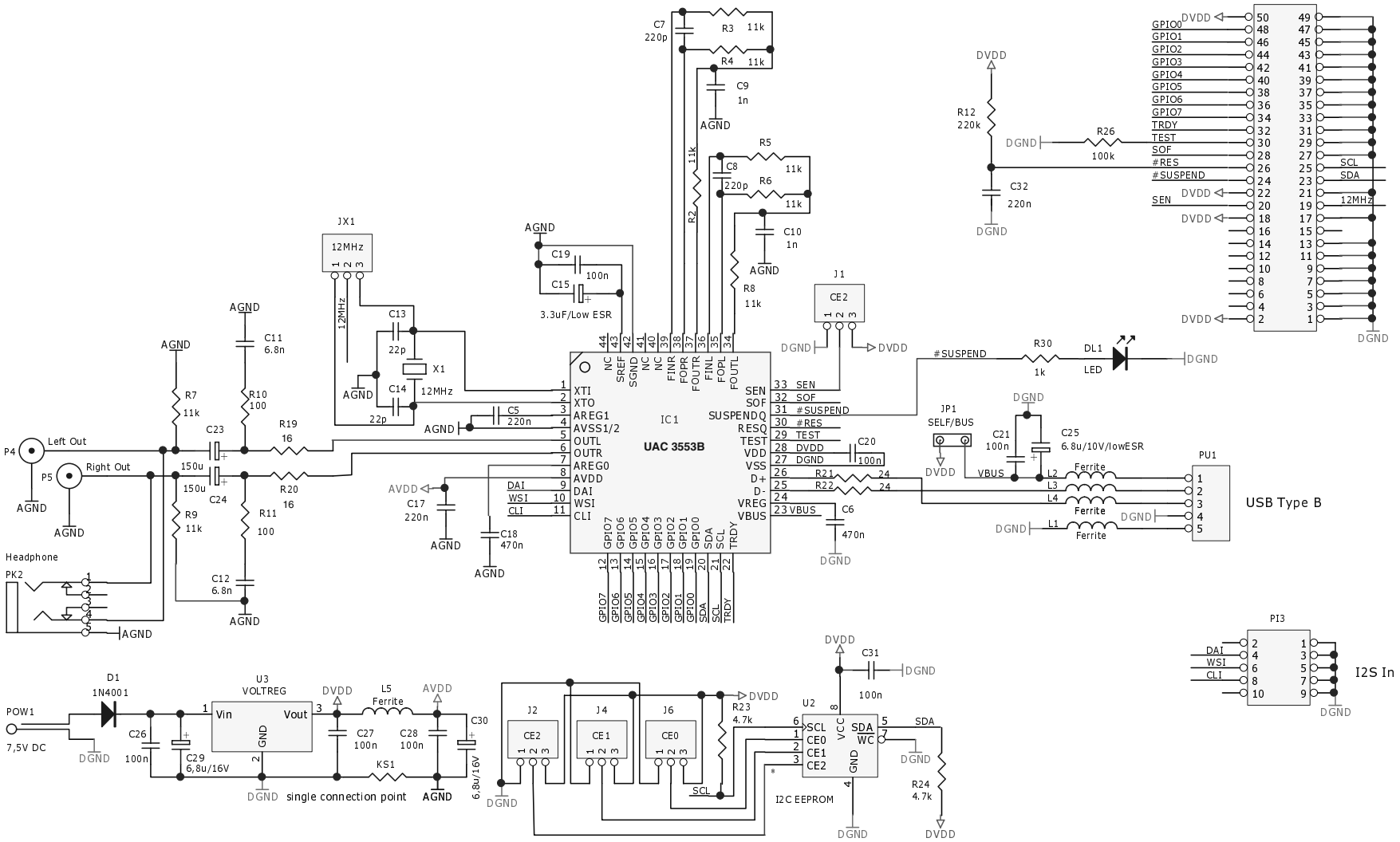


Fig. 6–2: Circuit for a typical UAC application

7. Data Sheet History

1. Data Sheet: “UAC 3553B Universal Serial Bus”, May 21, 2003, 6251-595-1DS. First release of the data sheet.
2. Data Sheet: “UAC 3553B Universal Serial Bus”, Feb. 17, 2005, 6251-595-2DS. Second release of the data sheet. Major changes:

– Section 3.1. on page 13 “Sample Rate Converters” was added.

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